Fabrication of the GLAST Silicon Tracker Readout Electronics

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***Abstract*—A unique electronics system has been built and tested for reading signals from the silicon-strip detectors of the Gamma-ray Large Area Space Telescope mission. The system amplifies and processes signals from 884,736 36-cm long silicon strips in a 4×4 array of tower modules. An aggressive mechanical design fits the readout electronics in narrow spaces between the tower modules, to minimize dead area. This design and the resulting departures from conventional electronics packaging led to several fabrication challenges and lessons learned. This paper describes the fabrication processes and how the problems peculiar to this design were overcome.**

***Index Terms*— Application specific integrated circuits, Astronomical satellites, Cables, Fabrication, Multichip modules**

I. INTRODUCTION

The Large Area Telescope (LAT) of the Gamma-ray Large-Area Space Telescope (GLAST) mission [1] is a pair-conversion gamma-ray detector designed to carry out research in high-energy astrophysics and particle-astrophysics. It is scheduled to be launched into low-Earth orbit by NASA in late 2007. The tracker-converter of the LAT is an array of 16 detector modules [2][3], each in the form of a tower of 19 stacked "trays," one of which is depicted in Fig. 1. A tray is a stiff, lightweight carbon-composite panel that supports the tungsten foils, which serve to convert the incoming gamma-ray into an electron-positron pair, and the silicon-strip detectors (SSDs) that track the charged particles and reconstruct the direction from which the gamma-ray arrived. The readout electronics for the SSDs are multi-chip modules (MCM), which are mounted on two edges of each tray, as illustrated in Fig. 1. A right-angle interconnect, in the form of a single-layer flexible circuit, carries the signals and bias currents around the corner of the tray to connect the SSDs to the MCM.

Each MCM supports the readout of 1536 silicon strips. It consists of a single printed wiring board (PWB), illustrated in Fig. 2, upon which are mounted 24 64-channel amplifier-discriminator chips (GTFE) and two digital readout-controller chips (GTRC), the right-angle interconnect, bias and termination resistors, decoupling capacitors, Tyco/Raychem resettable fuses, and two Omnetics nano-connectors. See Fig. 3 for a photograph of one end of an MCM mounted on a tray. Each nano-connector plugs into a long 4-layer flexible-circuit cable, each of which interfaces 9 MCMs to the data-acquisition electronics located below the tracker in the Tower Electronics Module (TEM).

The requirements, design, and performance of the readout system are described in [4]. Some early experiences in the production of the MCMs can be found in [7]. Here we describe in more detail the MCM fabrication process and report on the full production experience. We also report on the fabrication of the flexible-circuit cables.

II. MECHANICAL AND THERMAL REQUIREMENTS

The MCM and its interconnects were designed to meet several mechanical and thermal requirements in addition to the functional and radiation-hardness requirements discussed in [4]. The circuit board must be compact and located on the edges of the trays, in order to minimize dead space between tower modules, and at least 99% of the channels in the system

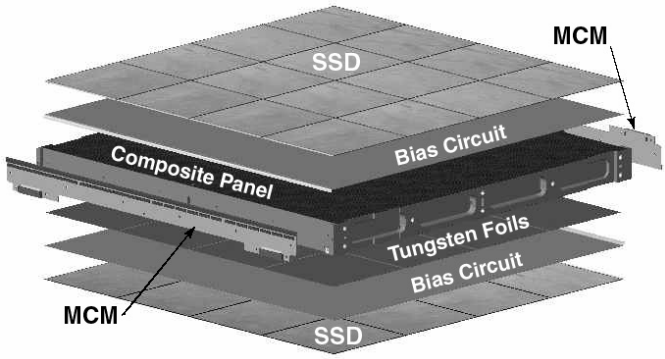

Fig. 1. Exploded view of a tray assembly from the middle of a tower module (the top and bottom trays have SSDs on only a single side, and the lowest three trays have no tungsten).

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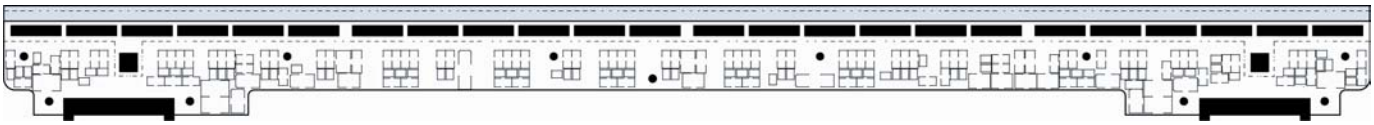

Fig. 2. Scale drawing of the MCM. The 26 chips, the two connectors, and the mounting holes are shaded black. The raised region of the PWB, where the pitch-adapter flexible circuit is bonded, is lightly shaded. The dashes delineate the limit of the region encapsulated in epoxy. The overall length is 35.9 cm.

must be functional. The system must survive repeated temperature cycles between −25°C and +60°C, and it must survive a GEVS [6] random-vibration spectrum with a total rms acceleration of 14 g. The materials must conform to strict NASA outgassing requirements, and the parts must be approved for space flight.

Most of the unorthodox aspects of the mechanical design of the tracker readout system were driven by our desire to minimize the dead space between tower modules. In the final design, the distance from the detector edge in one module to the detector edge in the adjacent module is only 15.9 mm. That includes the 2.5 mm gap between modules and the 1.5 mm thickness of each of the two carbon-composite sidewalls. The space in that dimension allocated to each electronics module is only 4.2 mm. Therefore, the MCM must be mounted at a right angle to the SSDs, complicating the interconnection between the amplifier chips and SSDs.

Fig. 4 shows a scale cross section of the tray edge where the MCM resides. The thermal boss is part of the carbon-carbon closeout onto which the MCM is mounted. The ~0.25 W of heat generated by the electronics flows through the thickness of the MCM, through the Scotch-Weld 2216 epoxy adhesive bonding the MCM to the closeout, and then through the carbon-carbon material and into the carbon-composite sidewall, which carries the heat to the bottom of the tower module. While the ~7°C temperature drop in the tower-module sidewalls from top to bottom was a major driver in the tower-module design, the temperature drop from the ASICs through the PWB and the bonded joint is comparatively insignificant. Therefore, cooling considerations never constrained the design of the MCM itself.

Fig. 4 shows that wire bonds from the MCM to the SSDs are applied to the narrow edge of the MCM. To apply successfully 1552 wire bonds along that edge, the surface should be as flat and straight as possible, and the MCM must be aligned accurately to the tray. Issues associated with this process are discussed in Sections IV and V.

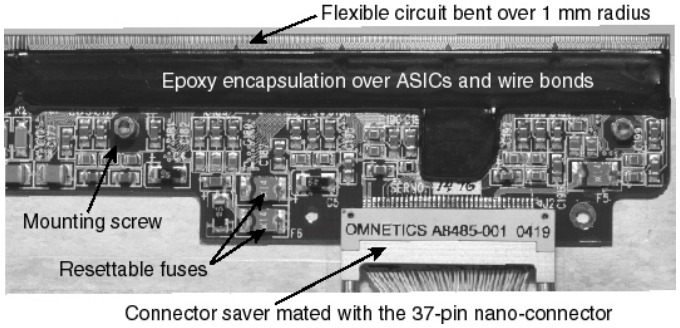

Fig. 3. View of approximately ¼ of an MCM, mounted in an aluminum carrying case.

III. ASIC Testing and Dicing

The 64-channel amplifier-discriminator ASIC (GTFE) and the digital readout-control ASIC (GTRC) were fabricated in the Agilent AMOS-14 CMOS process on 6-inch wafers. They were tested on the wafer using an automated probe station. On each chip, all I/O pads were simultaneously probed except for the 64 amplifier input pads of the GTFE chips. The amplifiers were tested by way of the internal charge injection circuitry. The test suite included power measurements and exercised all of the digital functionality in both chip types. GTFE chips were not accepted if even a single amplifier channel tested bad.

The GTFE test yield was 94.9% with a standard deviation of 4% for 181 wafers tested, with 181 chips per wafer. The GTRC test yield was 87.6% for 19 wafers, with 297 chips per wafer. The bad chips were automatically marked by an ink jet.

The large number, 26, of chips on the MCM put a premium on starting the assembly with only known good chips. Bad chips resulted in expensive debugging and rework. It was crucial to avoid damage to the chips between the wafer test and the delivery to the MCM assembly vendor [8], as it was not possible to retest the loose chips after dicing. The wafers were lapped to a thickness of 270 μm before dicing [9]. There was no metal plating on the back side. The good dice were inspected by automated optical equipment after picking from the wafers and then were shipped in Gel-Paks, which avoided damage from chips rattling around and also easily accommodated the large size and odd shape of the GTFE chip (13 mm by 2.5 mm).

The automated inspection rejected about 8% of the chips, almost all because of scratches, according to the data supplied by the dicing vendor. However, after further investigation, we learned that in most cases the optical comparators rejected the chips because of irregularities in internal probe pad outlines, and the scratches were made by the vacuum wands that picked up the rejected chips. Apart from the unnecessary loss of up to 8% of the chips, this process was successful in the sense that the incidence of MCM debugging and rework, about 1 in 10 MCMs, was acceptable and was dominated by factors other than bad chips. The most common test failures were missing wire-bond connections, which were easy to isolate and fix (see Section VII).

IV. PWB

The PWB has 8 layers of traces and planes (½ oz. Cu), separated by 75 to 100 μm of polyimide-glass dielectric (Arlon 35N), except that the top two signal-trace layers are separated by twice as much dielectric to reduce the capacitance of the signal traces. Except for the raised edge, the fabrication was standard technology [10], but with an oddly shaped and rather crowded board. The minimum conductor spacing is 100 μm (4 mils), and the internal pads are 500 μm (20 mils) in diameter. Complete annular rings of 50 μm (2-mils) minimum width were required on all internal via connections. The outer layers were plated with 0.25 μm (10 μ-inch) of gold over 4 μm (150 μ-inch) of nickel. The top was protected by a standard green solder mask, but the back side was covered with a bonded sheet of 50-μm Kapton, for electrical isolation of the 100 V SSD bias potential.

The long, narrow raised edge was formed by a technique designed to maintain a straight edge and tight dimensional tolerances. During fabrication, each panel contained 5 PWBs. A second panel of the same size and made from the same polyimide glass (but with no copper) was prepared with a rectangular cutout over the location of each MCM. The two panels were aligned by pins and bonded in a press, using an acrylic adhesive. When the 5 MCMs were then routed out of the bonded panels, all that remained on the MCMs from the second panel was the narrow strip along the MCM edge. At that point the edge was not yet rounded and the MCM was slightly oversized.

The completed PWBs that passed all electrical tests and coupon evaluations were sent to a machine shop to mill the raised edge to the final height and required straightness and to form a 1 mm radius. To ensure a smooth transition from the radius to the straight edge, a custom cutting tool was made that cut the radius and the flat edge simultaneously. At the other end of the 90° radius the tool was designed to leave a discontinuity in slope of about 3° to allow for ample tolerance in setting the depth of the cutter. The precision machining was important in order to avoid cracking the flexible-circuit traces when bending them around the edge and to ensure a uniform edge for wire bonding between the SSDs and the MCM.

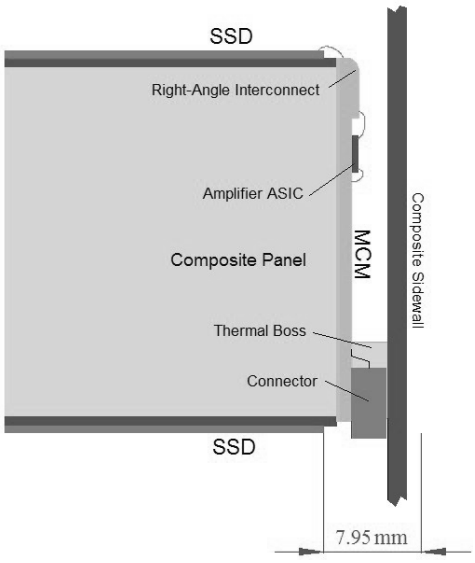

Fig. 4. Cross section at the end of a tray, showing the small gap in which the MCM is mounted between tray and sidewall. The dimension line is from the SSD edge to the midpoint between adjacent tower modules.

In general the PWBs performed well, except for several boards that formed short circuits between the 7th and 8th layers. Those are the two layers with the bias potential between them, and both layers include large planes of copper. The short circuits formed at points well away from the plane edges and well away from any vias. They were rare, never occurring during preproduction testing, and were not found until the completed MCMs were operated at 100 V in the 85°C burn-in chamber, usually in the first 24 hours of the 168-hour burn-in. Despite a lot of effort in destructive physical analysis, the root cause was never completely understood, but the short circuits were shown to be associated with minute impurities embedded in the prepreg.

The bias potential is operated at 100 V on all towers, which is enough to ensure >99.5% detection efficiency for minimum-ionizing particles passing through the SSDs at normal incidence. However, since the supplies can be set as high as 120 V, strictly speaking the dielectric thickness should have been 200 μm thick, as recommended by IPC 2221 [5] for the 100 V to 150 V range. Instead, as part of an effort to squeeze the electronics into the allocated space, the design called for 100 μm thick prepreg, formed from two layers, which conforms to the IPC recommendations for the range 50 V to 100 V. The dielectric strength of the materials is far more than sufficient at that thickness, and the design was accepted by engineering review. But as we found out, contaminants can cause failures even at 100 V or less.

Microscopic examinations done after the first short circuits were encountered showed that in reality the first runs of boards had only a single layer of prepreg between those layers, which was squeezed down to 75 μm thickness. We then had the manufacturer change their process to conform to the two layers specified in the drawings. Some shorts nevertheless formed in boards from the revised process. By that time in the project the entire original margin in space had been used up elsewhere, and insufficient room and schedule-time remained to remanufacture the boards with double the dielectric thickness. Nevertheless, no failures were ever seen after completion of the MCM burn-in or in the last ¼ of the burn-in period. The burn-in process was successful in screening out the bad boards, albeit only after they had been fully assembled. Long term failures cannot be ruled out, but any single short circuit would result in the loss of only 1 out of 2304 detector ladders, consequently with negligible degradation of the instrument's scientific performance.

V. Right-Angle Interconnect

The right-angle interconnect between amplifier chips and SSDs is made from a single-layer flexible circuit, which is bonded over the 1 mm radius machined into the fiberglass PWB. The tight space constraints made every aspect of this process a challenge.

The flexible circuit is covered by 1536 signal traces and 16 SSD bias traces, which are roughly parallel but jog slightly to conform to the SSD strip pitch, which at 0.228 mm is slightly larger than the 0.20 mm amplifier pitch on the ASICs. The ends of the ½-oz copper traces must be plated with nickel and thin gold for aluminum wedge wire bonding. To avoid plating the bend region we tried covering it, experimenting first with a Kapton cover layer and later with a flexible solder mask. In both cases the combined tolerance of the cover application and the process of bonding the circuit to the MCM made it impossible to guarantee that all of the wire bonding areas would be uncovered while, at the same time, the edge of the cover would not be within the bend region.

In the end we did not use a cover layer, and we plated the entire surface of the traces. That simplified the bonding process, but the nickel plating had a tendency to crack when bending the circuit. The cracks in the nickel were likely to propagate through the copper. Cracking was never eliminated, but it was kept down to a level of less than 4 cracks per 10,000 traces, which was acceptable. The nickel plating was about 4 μm thick, and the gold was about 0.25 μm thick. The plating must be done electrolytically. When we tried bonding some circuits that had been plated non-electrolytically by error, nearly 100% of the traces cracked during bending.

The flexible circuit was made oversized, with alignment holes around its perimeter. Custom tooling was built to bond the flexible circuit to the PWB. Fig.5 illustrates the tooling concept used to mold and bond the flexible circuit around the radius on the PWB, and Fig. 6 is a photograph of one of the tools, shown during the bonding process just prior to clamping the mold into place. The tooling worked well in terms of minimizing stress on the circuit during bonding and in making a good bond while maintaining a straight edge where the wire bonds are made from the SSDs to the MCM. Due to the inherent stiffness of the flexible circuit, the process tended to squeeze too much epoxy out of the region of the radius while maintaining a good bond thickness near the edges. This did not cause any structural problems but did result in the flexible circuit not being perpendicular to the back of the PWB, such that the wire bonder making the connection from SSD to PWB had to wire bond to a surface that was sloped by a few degrees.

Scotchweld 1838 green epoxy was used for bonding the flexible circuit, cured at 80°C for 1.5 hours. It has a paste-like consistency and good squeeze-out and temperature properties. The two components were degassed prior to dispensing them through a mixing tube. The Kapton surface was prepared by lightly abrading with 400-grit paper and cleaning with alcohol and acetone. A motorized screen printer and metal template were used to apply a controlled thickness of epoxy to the flexible circuit.

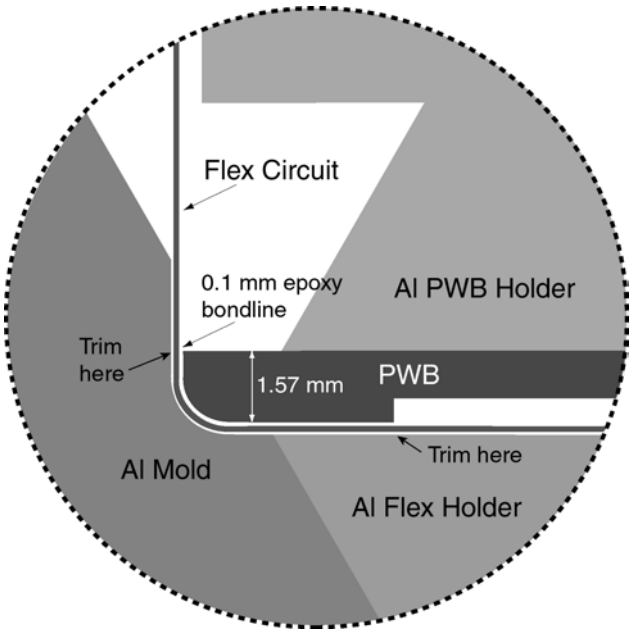

Fig.5. Detail of a transverse cross section of the tooling used to bond the flexible circuit to the PWB, magnified to show just the region where the bond is made. The tool consists of an aluminum holder for the PWB, another piece that holds the flexible circuit, and a mold piece that bends the flexible circuit over the radius in the PWB. After curing the adhesive, the assembly is removed from this tooling and the excess of the flexible circuit is trimmed off at the two indicated locations.

The flexible circuit was trimmed along both long edges after bonding, using a cutting wheel guided along two steel rails. It proved to be difficult to cut the circuit flush with the back of the PWB without sometimes cutting into the fiberglass, mainly because it was not easy to hold the edge of the PWB precisely straight. Tightening screws into the mounting holes was not sufficient—the PWB had to be clamped between two pieces of metal as close as practical to the edge where the trimming took place. Trimming the opposite edge (next to the chip locations) frequently resulted in cutting into the fiberglass of the riser, because of variations in the location of the riser edge, but that was not a serious problem. The epoxy encapsulation covered that region and

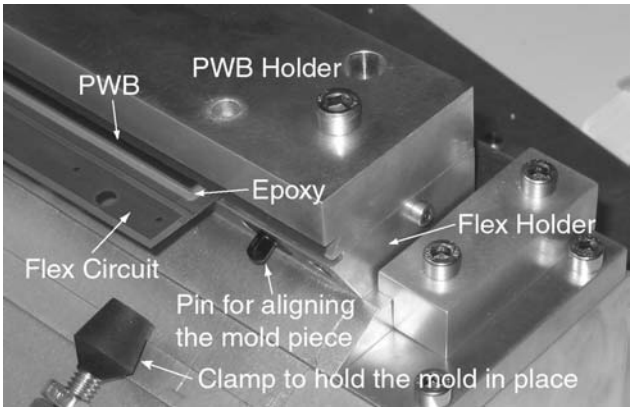

Fig. 6. Photograph of the tooling used to bond the flexible circuit to the PWB, shown prior to installation of the mold piece.

firmly fixed any loose fibers in place.

During the remaining processing steps about 5% of the MCMs developed small, localized debonding of the flexible circuit along the trimmed edge. The edge under the encapsulation did not cause problems, but debonding as small as a millimeter or less along the other edge had to be manually repaired before wire bonding the SSDs to the traces along that edge. Other than those small delaminations, the precision of the PWB machining and flexible-circuit bonding was adequate for wire bonding between SSDs and MCMs.

VI. Soldering and Die Attach

The soldering of the surface-mount parts, except for the connectors, was done by infrared reflow. For application of the solder paste, it was necessary to make a special silkscreen to work around the raised edge of the board, which would interfere with a normal silkscreen. A Mydata TP9-2U pick-and-place machine loaded the SMT components on the board. The two connectors, which have surface-mount solder pins, were hand soldered after fastening them to the board with countersunk screws.

The long thin board could not go through the reflow oven without being fastened to a flat jig. The aluminum jig tended to act as a heat sink, so that had to be taken into account when tuning the temperature profile of the oven. On the other hand, the resettable fuses were temperature sensitive, requiring us to avoid excessive heating. Once the necessary temperature profile was determined, we had the manufacturer simulate the same temperature profile on all of the resettable fuses before measuring their properties and screening them. The profile had a duration of 12 minutes and a peak temperature of 210°C.

After using an automated dispenser to apply silver epoxy (Epo-Tek H20E) to the board, the 26 chips were placed manually. Use of automation for placing the chips would have required engineering and fabrication of special jigs to handle such an odd, long board, and that was not judged to be cost effective for this size production run.

Curing of the die-attach epoxy at 80°C induced stresses that tended to warp the MCM by up to a few millimeters in the long dimension, mainly because of a large mismatch in thermal-expansion coefficient (CTE) between the PWB and the silicon chips, which cover nearly the full length of the MCM. We managed that problem by keeping the MCM fastened to flat jigs during all fabrication and test procedures, as well as during storage and shipping. The flexing that took place when moving the MCM from one jig to another did not cause any problems.

VII. Wire Bonding

The MCM was plasma cleaned prior to wire bonding, and aluminum wedge bonds were made by a Delvotec 6400 automated wire bonder. Due to limitations in reach of the machine, each MCM had to be wire bonded in two sections. At the beginning of each production shift at least one GTFE chip was wire bonded on a reject part and the wires were destructively pull tested. On every 3rd MCM about 30 wire bonds were non-destructively tested. The wire-bonding program targeted the IC chip pads (90 μm by 200 μm) toward one side of each pad, to allow a second bond to be made to NASA specifications in case the first failed.

The wire bonds were visually inspected afterwards, and the MCM was put through an electrical test that could check all wire bonds except those going to the flexible circuit. Each MCM has 2816 wire bonds, and about 1 in 10 MCMs would initially fail the test, most often because of a lifted or missing wire bond. An expert had to be available daily on site or by email contact to interpret the test results and localize the bad wire bond. The failure rate initially was higher, and measures were taken to improve it, including plasma cleaning, handling improvements to avoid mechanical damaged to completed bonds, and improved programming and operator training done by an outside consultant. Nevertheless, the MCM remained challenging to wire bond, due to its large and awkward size, high number of bonds, and less-than-ideal bonding substrates on the PWB and flexible circuits.

The 1536 amplifier input connections to the flexible circuit and the 16 SSD bias connections could not be tested at this point. For them we relied on visual inspection. Each SSD bias connection had two redundant wire bonding pads, and we put two wires on each pad to give a 4-fold redundancy. The system requirements allowed up to 0.5% of the MCM channels to be non-functional, so we could afford to have an occasional bad wire bond between flexible circuit and amplifier.

VIII. Encapsulation

All chips and wire bonds on the MCM were encapsulated by a black epoxy (Hysol FP4450 and FP4451) using a dam-and-fill method. The epoxy makes a very close match in CTE to the transverse properties of the polyimide-glass PWB. However, the CTE of the polyimide-glass in the thickness direction is much greater. That is not normally an issue, but on the LAT tracker MCM the encapsulation covers the 0.55 mm vertical edge of the riser. That caused some concern that delamination might be induced by the differential thermal strain of up to 0.6% over the temperature range between cure (125°C) and the low point of our thermal cycles (–30°C). However, after initial contamination problems were resolved (see below) there was no further incidence of delamination.

The encapsulation was applied by a GPD automated dispenser, with the MCM work holder heated to 70°C. One bead of dam was applied along the flexible circuit, but two successive beads were necessary on the lower PWB substrate in order to build up the dam high enough to ensure coverage of all of the wires. The dam application was particularly difficult at the two ends of the board, due to insufficient clearance between the PWB edge and the first and last chips, and early on a few MCMs were rejected due to exposure of the last one or two wire bonds. The dam and fill were applied

in four sections, each containing 6 GTFE chips, but all encapsulation on an MCM was cured at the same time. Note that it was not possible to apply a second touch-up layer of encapsulation after even partial curing of the first layer. The second layer would not bond adequately to the first, and any flexing of the MCM would cause it to delaminate.

In a few MCMs the encapsulation procedure left a small air bubble below a group of wire bonds on the input side of the GTFE chips (the wire bonds with the closest spacing, at 200 μm pitch). When the epoxy was cured at 125°C, the expanding air would blow a tiny hole out of the top surface, leaving a small cavity in the encapsulation. Those MCMs were accepted as is, since the encapsulation was judged to be still providing adequate mechanical protection to all of the wires.

In a few percent of the MCMs the encapsulation procedure would break one of the wire bonds from an IC chip to the PWB or from chip to chip, to be discovered in subsequent electrical tests. Probably those wire bonds were already defective and so weak that the flow of the epoxy broke them. Those MCMs had to be discarded.

In the early production there was a much larger incidence of breakage of signal wire bonds from the chips to the flexible circuit. Most of those breaks occurred during thermal cycling when the encapsulation delaminated from the Kapton/gold flexible-circuit surface, taking the fragile wires with it. We allowed up to 0.5% of the input channels to be broken in this way on an MCM without rejecting the part, but delamination would typically break many adjacent wire bonds, and in the worst case 750 wire bonds were broken! After an investigation we concluded that the problem was due to silicone contamination. We discovered that the flexible-circuit traces had been covered by a Kapton tape with a silicone-based adhesive, applied by the assembly vendor before abrading and bonding the flexible circuit, in order to protect the plated traces. The silicone-based adhesive violated NASA regulations and was noticed by a NASA quality engineer during an on-site inspection. The offending tape had remained in place through completion of the reflow soldering process, and the pre-wire-bonding cleaning with an alcohol-acetone mixture and then with plasma apparently did not always remove enough of the adhesive residue. After replacing the tape by a different Kapton tape with acrylic adhesive the delamination problem never recurred.

IX. Conformal Coating

The top surface of the MCM was coated with Humiseal 1A20 to a thickness of 25 to 125 μm, except for the flexible circuit and the areas covered by encapsulation. The conformal coating would not adhere to the encapsulation epoxy, so it was necessary to mask the encapsulated areas before spraying the coating. The flexible circuit, the connectors, and the mounting holes also had to be masked.

The application was done manually, using a small airbrush. Meeting the NASA workmanship standards required a tedious technique of spraying each individual part from all 4 sides. Too much spraying resulted in excess thickness and small bubbles, while insufficient spraying could leave one side of a component uncoated. The conformal coating was inspected and touched up under an ultraviolet light.

Initially the spraying was done with connector savers mated to the two nano-connectors. That sometimes resulted in conformal coating wicking under the connector and then into the mating area, making a mess of the connector. Finally we had to remove the connector savers, mask the connector faces, and then reattach the connector savers after completion of the coating.

X. Electronics Module Testing

Two identical test systems were built for testing the MCMs. One was located at the assembly vendor and the other at SLAC. The test system interfaced to the two nano-connectors on the MCM. It exercised all of the digital logic in the GTRC and GTFE chips and all of the inter-chip communication. It also exercised all 1536 amplifiers by executing charge-injection scans, using the internal GTFE calibration system, and by measuring noise occupancy versus threshold setting.

At the start of production the test system could not verify the electrical connections from the flexible circuit to the amplifier inputs, so we could not detect broken connections until the MCM was permanently mounted on a tray and wire bonded to the SSDs. On a few MCMs those connections were verified by probing with an automated probe station, but that was very tedious and slow and could not be done at the assembly vendor. Eventually we implemented a simple and effective solution employing a jig that supported the MCM and clamped a long Fujipoly Zebra elastomeric connector against the full length of the flexible circuit. The opposite side of the Zebra connector was pressed against a ground wire. With this setup we could reliably connect all of the flexible-circuit strips to ground, at which point we ran a charge-injection routine on all channels. An amplifier with its input connected to ground will test dead, so any amplifier that responded to the charge injection was identified as being disconnected. False negative results were possible if the Zebra connector failed to make contact with a trace on the flexible circuit, but the incidence of such false negatives was low enough not to be a problem. False positive results sometimes resulted when the pressure of the Zebra connector against the flexible circuit temporarily reestablished a broken connection. The rate of false results was checked by repeating the test, which took only a few seconds to execute, with varying pressure and with the jig's Zebra connector shifted by about 0.5 mm to the left or right. The test was fast and very effective at identifying cracked traces on the flexible circuit or broken wire bonds to the amplifier inputs.

The MCMs were tested twice at the assembly vendor, once before encapsulation of the wire bonds and once just before shipping to SLAC. At SLAC each MCM was subjected to 20 thermal cycles between –25°C and 60°C, followed by a

functional test at each of three temperatures: –25°C, 25°C, and 60°C. Then each MCM was burned-in at 85°C for 168 hours, with a suite of functional tests executing repeatedly. The test system used for these tests and the burn-in was based on the LAT data acquisition system and could handle up to 36 MCMs simultaneously (a full tower-module). Dry nitrogen was used to avoid condensation in the chamber during the thermal cycles.

The standard burn-in temperature specified for integrated circuits is 125°C, but we could not exceed 85°C without risking damage to other components, in particular the resettable fuses. Since all tracker chips run at very low power levels (the average temperature rise in a chip when powered is less than 1°C), and because of the high level of redundancy in the system, we were allowed to reduce the burn-in temperature. No circuitry ever failed during burn-in except for the PWB short circuits discussed in Section IV. None of the 15,912 IC chips has failed to date during operation of the 17 completed flight tower modules, including their thermal-vacuum cycles.

Following burn-in, each MCM was tested again on the single-MCM system, as only it could execute a comprehensive test, including the test of amplifier input connections, measurement of all LVDS quiescent levels, and cycling through the full address space. Completed MCMs were shipped to Italy for integration with the tray and SSDs. In Italy they were tested upon reception, with a system based on the LAT data acquisition system, and again after mounting onto trays, at which point it was possible to measure the noise performance with the full capacitive load attached and to measure signals from cosmic-ray particles.

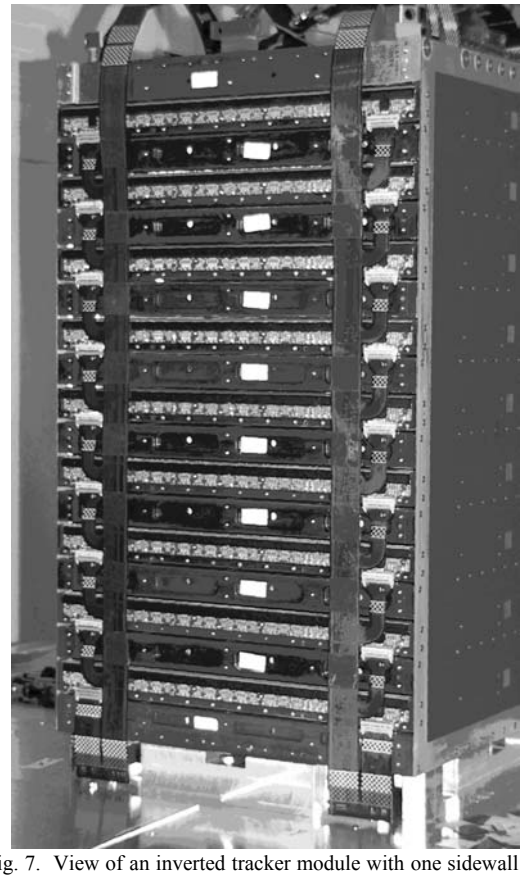

Fig. 7. View of an inverted tracker module with one sidewall removed, showing two cables and 9 MCMs.

Note that 50 preproduction MCMs were manufactured, burned-in, and tested prior to commencement of the flight-electronics production. In addition, five were subjected to an additional burn-in of 1000 hours, and five others were subjected to an additional 200 thermal cycles. However, neither the PWB short circuit problem nor the encapsulation delamination problem occurred in any of the preproduction units.

XI. Cable Fabrication

The tracker readout cables proved to be difficult and expensive to produce. They are 4-layer flexible circuits, with two layers of traces and two ground/power planes. One layer of traces routes MCM signals from the nano-connector on each of the 9 arms to the busses running the length of the cable on the other trace layer. Each of the 8 cables on a tracker module is a different layout, two of which can be seen in Fig. 7.

The minimum trace width and separation are 200 μm (8 mils). The pad diameter is 750 μm (30 mils). NASA tested coupons at opposite ends of each panel and required 50 μm (2-mil) minimum annular rings on inner as well as outer layers, with no voids allowed between trace and barrel. Those parameters are well suited to standard technology for circuits of normal size, but the tracker cables range from 84 cm to 98 cm in length. Most of the longest cables were made diagonally across a 91 cm (36-inch) panel, with only a single cable per panel. To add to the difficulty, the center dielectric layer, between the traces and the power plane, was double thickness (about 200 μm), to control the impedance of the LVDS signal pairs.

For schedule reasons, two independent manufacturers [11] contributed to the cable production, and both had difficulties with registration of the layers over the long cable length. Both manufacturers found it to be necessary to adjust the drill program panel by panel, based on *x*-ray images of test drillings made on each panel. Both manufacturers also achieved the best results by etching the two inner layers simultaneously, on a single substrate, and then drilling prior to etching the outer layers, using the adjusted drill program to adjust the etching accordingly.

The cable assembly included soldering of the surface-mount nano-connectors, the through-pin micro-D connector, two thermistors, and several surface-mount resistors. The exposed pins on the nano-connectors and the thermistors were potted with epoxy (Hysol EA-9394), and other exposed conductors received a conformal coating (Humiseal 1A20). The cable region around the micro-D connector was reinforced by a 0.8 mm thick piece of fiberglass.

The nano-connectors were bonded to the cable with a 0.13 mm thick film adhesive (Cytec FM-73M) prior to soldering. The adhesive was precut to match the nano-

connector shape. It was important to have adhesive under the aluminum wings holding the jack screws, as well as under the polymer molded part of the connector, to help prevent separation of those two parts during handling. However, the precut shape also had to be finely tuned to avoid squeeze-out onto the jack screws, solder pins, and mating surface. The connector body had a tendency to crack between the mating pins from the clamping force used during bonding, requiring special care and thorough inspections under microscopes. Some connectors with hairline cracks between a few pins were nevertheless used in the flight hardware, but only after much extra testing and discussion.

All of the bare flexible circuits were tested at 250 V for continuity and insulation prior to assembly. The completed assemblies were tested at low voltage by cable scanners after interfacing with nano-connector pigtails. Special care had to be taken to avoid connectors going bad in the test system and then spoiling connector pins on good cables. In general, the nano-connectors were fragile and had to be carefully protected by special covers to avoid bending of pins. A final test of each cable was made after reception from the vendor by connecting a cable pair to a set of 9 MCMs and a TEM and executing a suite of tests to simulate all aspects of the data acquisition, including measurement of the leakage current of the detector bias supply. Thermal-vacuum and vibration environmental acceptance tests were done only after installation of the cables onto the tower modules, but no failures were encountered there.

XII. Conclusion

Even though chip-on-board manufacturing is a well established technology, the tracker MCM is unusual in its size and for the large number of chips on it, and especially because of the right-angle interconnect needed to interface it to the SSDs. These factors made the fabrication more difficult than anticipated. The readout cables were also difficult to fabricate, because of their length and small features. Both MCMs and cables could have been designed to be more easily fabricated by increasing the space and material between tower modules, but the mechanical design was frozen well before the electronics fabrication problems were encountered.

Despite the problems encountered, the LAT tracking system was completed and performs extremely well, with all IC chips functional. All of the tracker tower modules passed their environmental tests. The vibration testing never caused any problems or loss of working channels. The thermal-vacuum testing did cause some insignificant losses in MCM regions already known to have small delaminations of the encapsulation, due to the contamination problems discussed above. The installed flexible-circuit cables and nano-connectors have performed flawlessly.

Based on the 2nd through 17th tower-module manufactured, the number of dead channels is only about 0.2% overall, with the majority of those due to the encapsulation problems. That leads to a detection efficiency of greater than 99.4% per SSD layer for minimum-ionizing particles. The power consumption meets the target of 160 W, with less than one in a million channels having noise hits per system trigger. See [4] for more details of the system performance.

Because of its aggressive electronics packaging design, the tracker achieves a remarkably high percentage of live area for such a large system: 89.4%. Achieving that goal required us to overcome many manufacturing challenges but will pay off in terms of an angular resolution for gamma-ray detection that is greatly improved with respect to previous generation detectors.

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