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SEE test of the LAT Tracker Front End ASIC

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Abstract

Single-event effects (SEEs) on the LAT front-end ASIC were tested using the "Top5" test chip in the SIRAD irradiation facility of INFN Legnaro on July 21–22, 2001. Heavy-Ion beams with a LET of 2.8–85.6 MeV cm^2 mg^{-1} were irradiated in the test. No SEL (single-event latchup) event was observed throughout all the irradiation tests. On the other hand, a number of SEUs (single-event upsets) in shift register blocks were detected, and the cross sections of the SEUs were obtained for each design block of the shift register and each 0-to-1/1-to-0 upset mode.

1 Experimental setups

1.1 Test chip "Top5"

Test chip "Top5", made in the Agilent/HP 0.5-μm process (AMOS14), was utilized for SEE tests of the LAT tracker front-end ASIC. The chip includes both analog and digital sections. The analog section consists of three channels of preamp, shaping amp, and comparator for TRK and one preamp for CAL. They are powered by two power lines of AVDD(2.5V) and AVDD2(1.5V). The digital section consists of a 128-bit shift-register powered by DVDD(2.5V). The 128-bit shift register is grouped into four blocks of 32-bit registers, each of which is designed differently: one of a normal Tanner-Tools SCMOS standard-cell design and three of custom SEU-resistive designs. We named the standard resister as REG#1, the SEU-resistive register designed by D. Freytag as REG#2, and the other two SEU-resistive registers designed by E. Spencer as REG#3 and REG#4. Table 1 summarizes the properties of the 128-bit shift register blocks. Also, Figure 1 shows the "Top5" chip layout and a schematic drawing of the shift-register blocks.

We tested for SEL (single event latchup) in both analog and digital portions and for SEU (single event upset) using the 128-bit shift register.

1.2 Heavy-ion beam of the SIRAD irradiation facility

SEE heavy-ion beam tests were performed on 21–22 July, 2001 at the SIRAD irradiation facility of the INFN Laboratori Nazionali di Legnaro [1]. Table 2 shows a list of ion-beam parameters used in this experiment, and Figure 2 shows a photo of the vacuum chamber involved in the ion-beam irradiation stage. More detailed information is shown in a test-log web page (`http://www.pi.infn.it/glast/tb/see/SEE_log_tab.html`).

Table 1: Summary of the blocks of the 128-bit shift register in the Top5 chip

Designation	bit-address area	SEU resistive?	Designed by
REG#1	0–31	No	Tanner standard
REG#2	32–63	Yes	D. Freytag
REG#3	64–95	Yes	E. Spencer
REG#4	96–127	Yes	E. Spencer

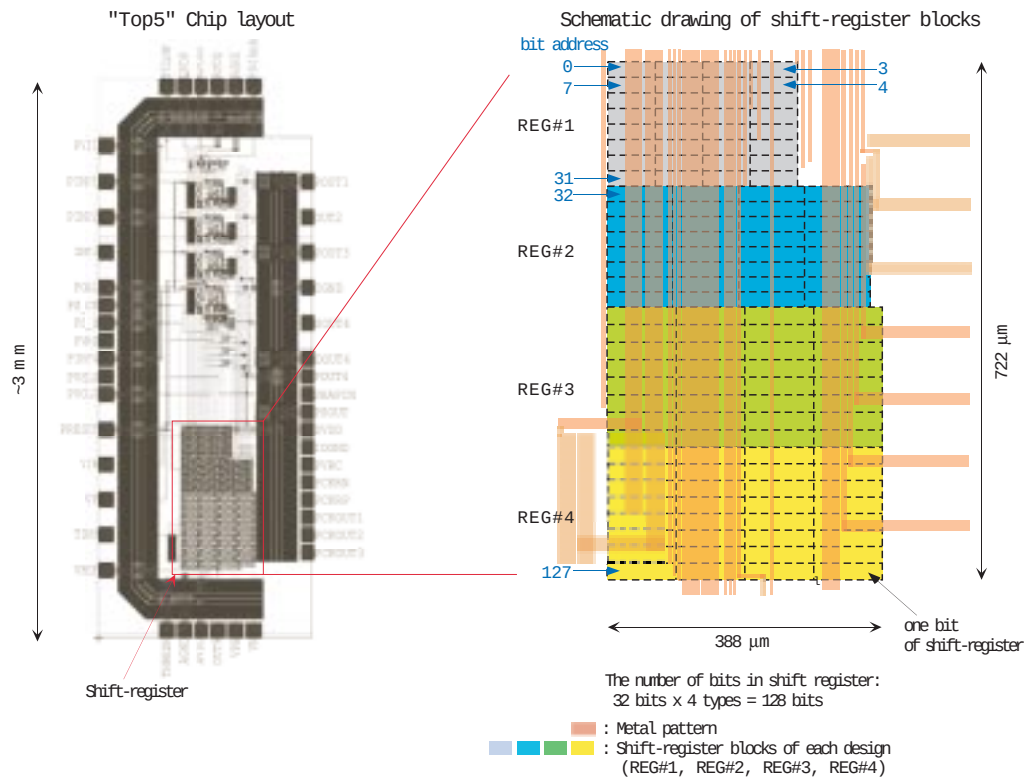

Figure 1: "Top5" chip layout and schematic drawing of the 128-bit shift-register on the chip

Figure 2: Photo of the ion-beam chamber.

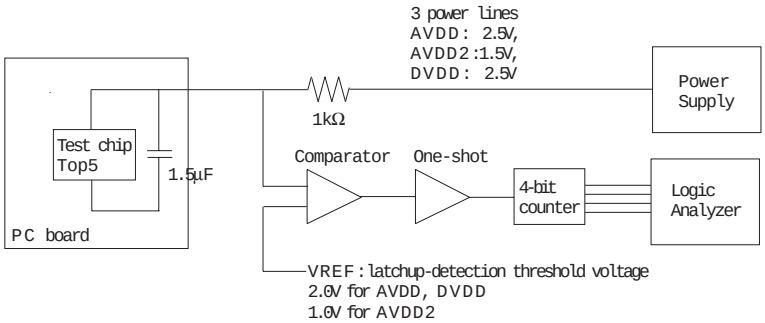

Figure 3: Schematic of lathchup detection curcuit

Table 2: Parameters of the ion beams for irradiation of each chip

Ions	Energy (MeV)	LET (MeV cm^2 mg^{-1})	Irradiation ion-fluence / dose (10^6 ions cm^{-1}/krad)			
			Chip ID	#1	#2	#3
^{16}O	112.06	2.81		—/—	30.0/1.35	30.0/1.35
^{24}Si	163.30	8.46		—/—	28.5/ 3.9	22.0/ 3.0
^{24}Si†	163.30	9.26		—/—	— / —	5.5 /0.82
^{58}Ni	239.43	27.4		—/—	9.0 / 3.9	13.6/ 5.8
^{128}I†	301.06	64.6		9.8/10	— / —	— / —
^{197}Au	275.68	78.17		9.5/11	— / —	— / —
^{197}Au†	275.68	85.6		—/—	— / —	8.0 / 11
			Total dose	/21	/ 9.1	/22.0

†: 21°-inclined irradiation

1.3 Test system

1.3.1 SEL detection circuits

We utilized the latchup detection circuit shown in Figure 3 to detect SEL and protect the chip for repeated operation in the beam test. The principle of the detection is as follows. If a latchup happens, it should draw large current from a power-line. We used a capacitor to provide the latchup current and a relatively large resistor to prevent a rapid current increase from a power supply. Thus, the voltage at the DUT (device under test) will rapidly go down and recover on a time scale of the CR time constant. The latchup detection circuit detects the voltage drop with a comparator. If the resistance is large enough, the latchup terminates when the current and the voltage decrease to less than the limits needed to hold the latchup.

We chose the resistor of 1 kΩ and the capacitor of 1.5μF there, taking into consideration the current needed to hold a latchup and the recovery time from a latchup. We also checked the circuit to work well using a latchup simulator prior the SEE test (appendix A).

1.3.2 Chip-control and data-acquisition system for SEU detection

We investigated the SEU probability by repeatedly writing a logic pattern into the 128-bit shift register, waiting a specified interval, and then reading it back. Figure 4 shows a schematic of the test configuration, including the chip-control and the data-acquisition system. We controlled the shift-register block with a logic analysis system, HP16500B, involving a pattern generator, HP16520A, and a state analyzer, HP16550A, which were operated by a remote PC via GPIB-ENET. We applied a logic pattern of a 128-bit sequence of 0101... to investigate a difference of the SEU cross sections between 0-to-1 and 1-to-0 upsets. Thus, the register bit addresses 0, 1, 2, 3, ..., 127 were set to 0, 1, 0, 1, ..., 1, and checked at the end of each time interval. We set the time interval to 5–10 s and tuned the beam flux such that the occurrence of SEUs was as many as a few per time interval for each 32-bit design block.

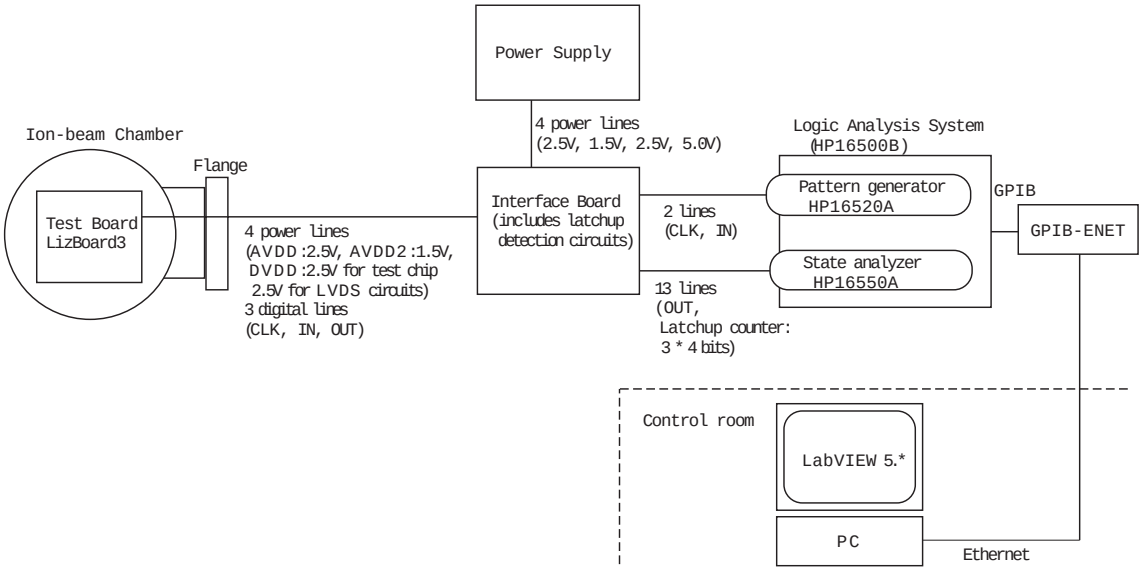

Figure 4: Configuration of test system at the INFN-LNL heavy-ion beam facility

2 Results and Analysis

2.1 SEL

No latchup was observed, indicating that the single-event latchup theshold is at least 86 MeV cm^2 mg^{-1} for the Top5 chip. This may be compared with the 63 MeV cm^2 mg^{-1} threshold measured by Osborn et al.[3] for the same CMOS process but with slightly different design rules.

2.2 SEU

We clearly observed SEU events in ion-beams with an LET higher than 8.46 MeV cm^2 mg^{-1}. No SEU was observed in oxygen-ion beams with an LET of 2.81 MeV cm^2 mg^{-1}. We analyze here the data in detail to derive the implications for GLAST of these results.

2.2.1 SEU occurrence for each individual bit

First, to confirm that nothing anomalous happened in the tests, we checked the number of SEUs for each individual bit. Figure 5 shows the number of SEUs observed during each ion irradiation in each register cell. It can be seen from the figure that the number of SEU occurrences is not always uniform within each design block. Especially, the REG#2 design, with a bit address of 32-63, shows vacancies of SEUs every two bits, which just represents a difference between 0-to-1 and 1-to-0 upset modes. Therefore, we investigated the uniformity of the number of SEUs in each design block for each upset mode, 0-to-1/1-to-0, separately. In that case, the hypothesis that the number of SEUs is constant in each design block is acceptable within a 95% confidence limit.

2.2.2 SEU cross section for each design block and each transition mode

We found that the observed SEUs can be grouped into those of each design block and each 0-to-1/1-to-0 upset mode. Thus, we next investigated SEU cross sections for each of these groups. Figure 6 shows SEU cross sections for these groups derived by accumulating the numbers of SEUs within each group. It shows clearly that no 0-to-1 upset happened in the REG#2 register. The difference between 0-to-1 and 1-to-0 upsets is also apparent in the REG#1 register.

Figure 7 shows the dependence of the SEU cross section on LET. We can see that the threshold LET for SEU is around 8 MeV cm^2 mg^{-1}. We note here that the tendency of the SEU cross section to decrease for LET above 64.6 MeV cm^2 mg^{-1} is probably not significant when systematic errors are considered (section 2.3.2).

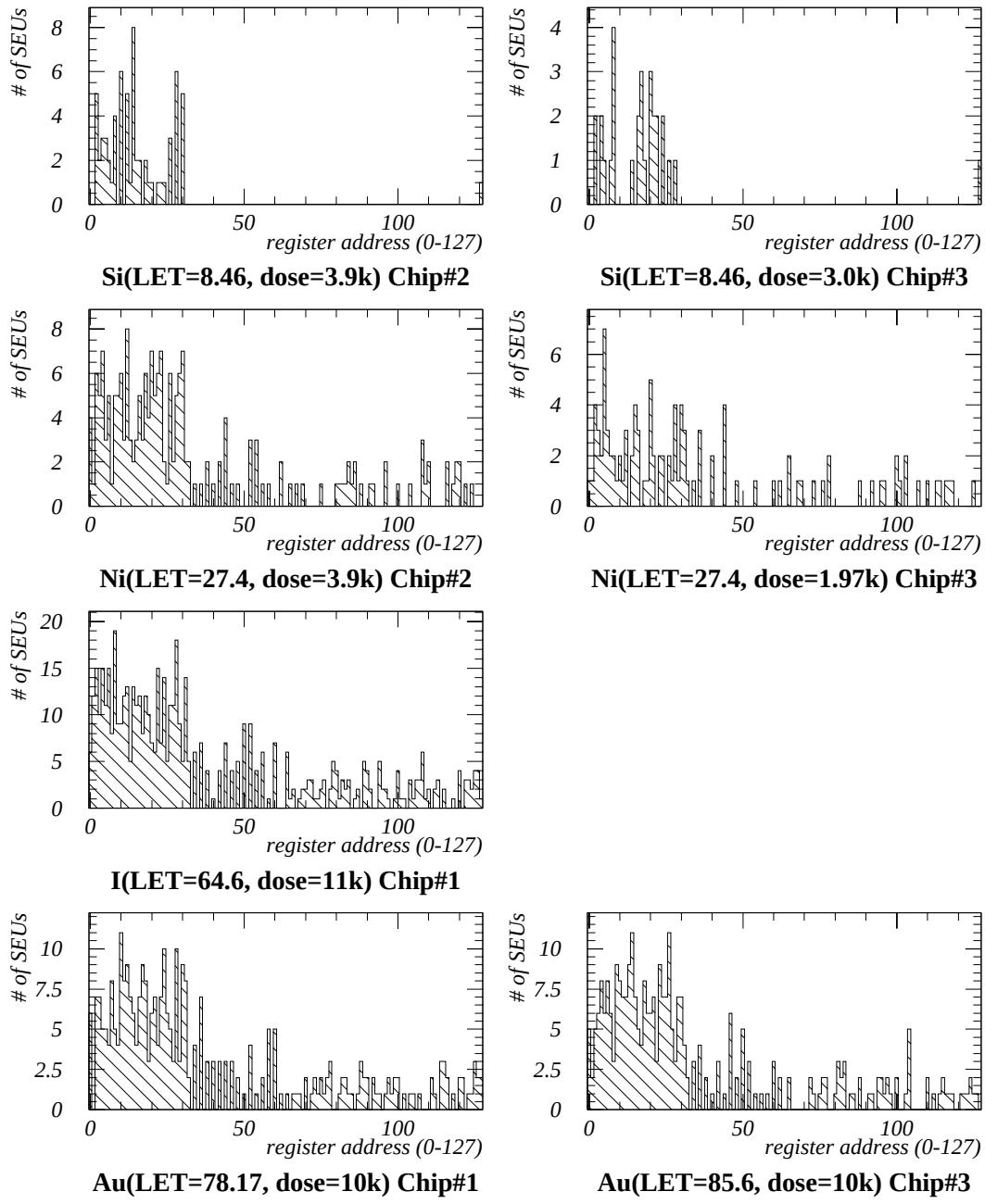

Figure 5: SEU occurrence in each individual cell of 128-bit-shift register block.

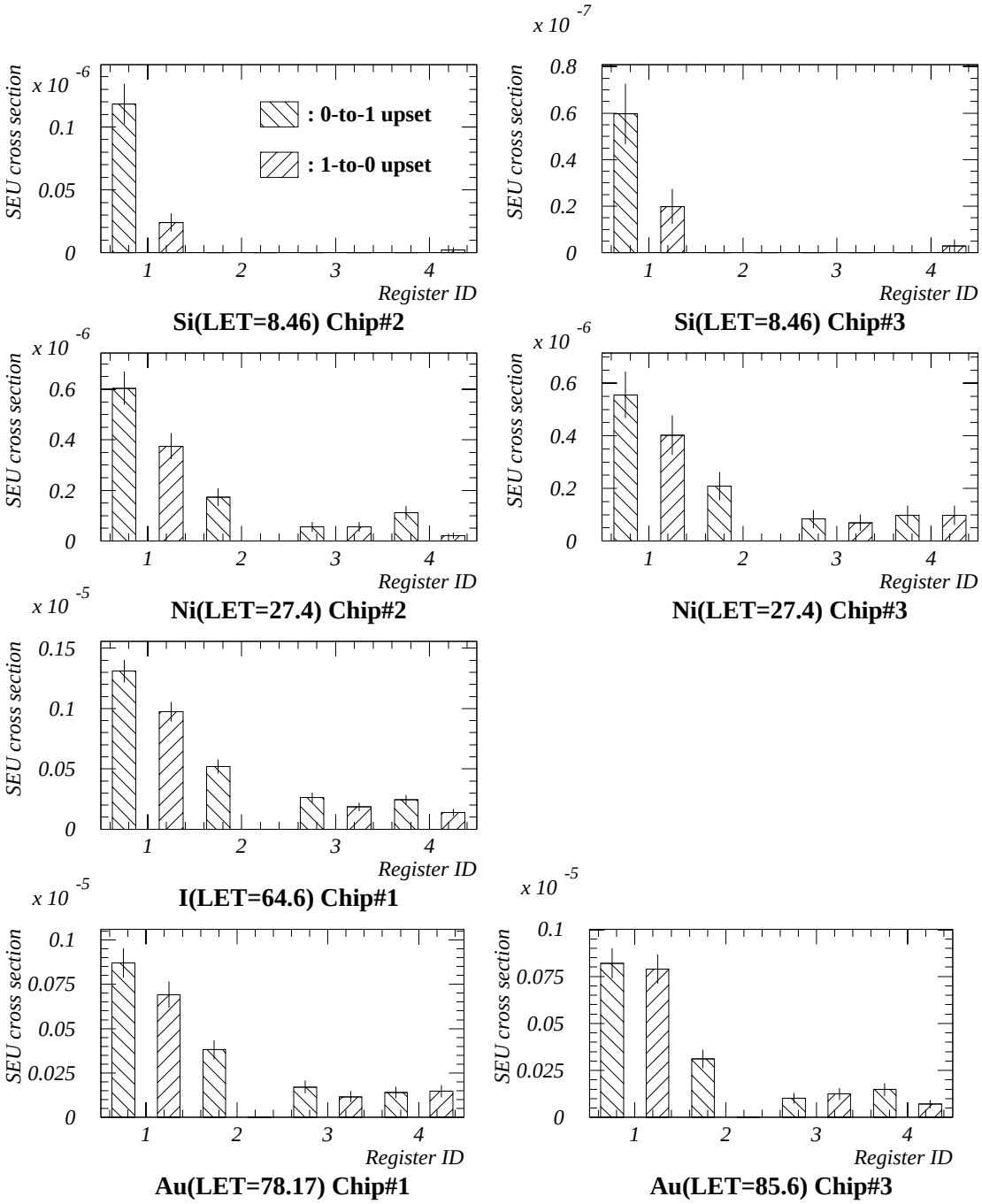

Figure 6: SEU cross section for each register design and transition mode:

- SEU cross section in y-axis is shown in units of [bit^{-1} ions^{-1} cm^2].
- Error bars represent the 1σ statistical errors.

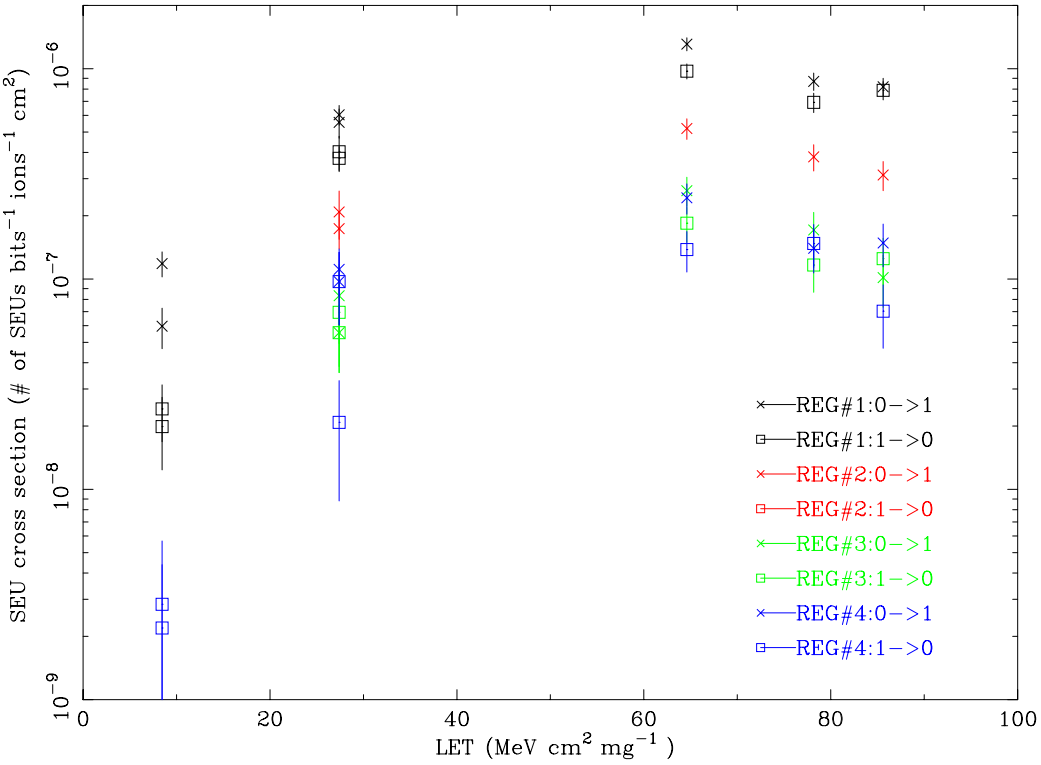

Figure 7: SEU cross section — LET relation

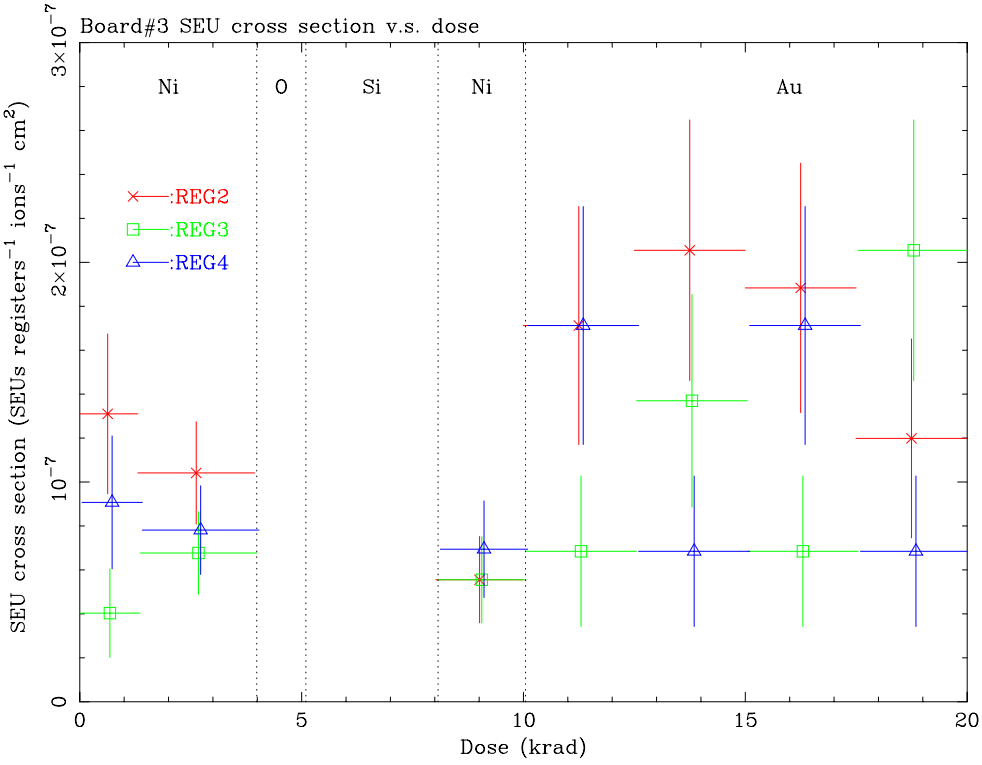

Figure 8: SEU cross section — dose relation

2.3 Validity check

2.3.1 Dose dependence of SEUs

It is not necessarily natural that the characteristic of the chip is unchanged throughout all of the ion-irradiation. In practice, although the chips on GLAST are expected to be irradiated by at most 10 krad in orbit, we irradiated the chips #1 and #3 by more than 20 krad for this test. Therefore, we check here the dose dependence of SEU occurrences. We use the data of REG#2, REG#3, and REG#4 on chip #3 during the irradiation of nickel and gold ions since their SEU cross sections show no significant LET dependence. Figure 8 shows the measured SEU cross section of chip #3 against accumulated dose, where SEU cross sections of 0-to-1 and 1-to-0 upsets are summed to gain the necessary statistical accuracy. The data are quite reasonable and no statistically significant tendency is seen. Thus, we conclude that we can treat all the data equivalently from the beginning to the end of the ion irradiation.

2.3.2 Systematic errors of the estimated fluences

We found that SEU cross section—LET relations (Figure 7) show a peak at a LET of 64.6 MeV cm^2 mg^{-1} and seem to decrease above that LET. It is contradictory to expectations. Therefore, we investigate these profiles in detail and consider the reasons for the discrepancy.

Figure 9 shows a plot of Figure 7 with a linear scale. The fitting analysis shows that only the data at 64.6 MeV cm^2 mg^{-1} are significantly high, given the statistical uncertainty.

In this test, ion fluences irradiated on the chip were estimated from count rates of four monitoring PIN diodes, which were positioned left, right, above, and below the test board. Ion fluxes at the chip position and at each monitoring PIN diode were measured during test-beam runs, and these ratios were utilized as flux correction factors to estimate the irradiated ion flux. Figure 10 shows the flux correction factors utilized in each ion beam. We can see that the factors at iodine beam seems to be anomalously high. Therefore, we think it is plausible that the data from the iodine beam have relatively large systematic errors, although we do not know any proper reason why such an anomaly happened in the iodine beam test. One difference between the tests is in a bias voltage of the monitoring PIN diodes; we changed it from 20 V to 50 V after the iodine test. However, it is hard to be considered as the reason because the pulses of the PIN diodes were

Table 3: Estimated SEU rate on the whole GLAST ASICs

Register type	SEU rate (#SEUs bit^{-1} day^{-1})		In the whole GLAST (#SEUs (1,893,888 bit) $^{-1}$ (10yr)$^{-1}$)	
	Galactic CR @Solar minimum	Solar event @worst day	Galactic CR @Solar minimum	Solar event @worst day
REG#1	2.05×10^{-8}	1.01×10^{-9}	142	6.96
REG#2	6.25×10^{-10}	1.30×10^{-10}	4.32	0.896
REG#3	1.35×10^{-10}	8.32×10^{-10}	0.93	0.575
REG#4	2.02×10^{-10}	9.13×10^{-10}	1.40	0.631

still well above threshold and fully efficient.

Anyway, except for the iodine beam, variations of the flux correction factors are smaller than the statistical errors of the SEU measurement.

3 Discussion

3.1 Consistency with the results of the pulsed laser test at NRL

Before the heavy-ion beam test at INFN Legnaro, we performed SEE tests using a pulsed laser, whose results are summarized in appendix B. Both results are mostly consistent:

1. No SEL was observed with an LET at least up to 600 MeV cm^2 mg^{-1} in the laser test.
2. No 0-to-1 SEU was observed in the REG#2 register block, for LET up to 433 MeV cm^2 mg^{-1}.
3. The threshold LET of a 0-to-1 SEU in the REG#4 register block, which is expected at 4.0 MeV cm^2 mg^{-1} from the laser test, are within 2.81–8.46 MeV cm^2 mg^{-1}.

However, there are also some slight inconsistencies:

a. No 1-to-0 SEU in the REG#3 register block was observed in the silicon-ion beam with a LET of 8.46 MeV cm^2 mg^{-1}. However, the laser test at NRL indicated the threshold LET at 5.3 MeV cm^2 mg^{-1}.

b. A lot of 0-to-1 SEUs were observed in the REG#1 register block in the silicon-ion beam with a LET of 8.46 MeV cm^2 mg^{-1}. However, the laser test indicated the threshold LET at 10.7 MeV cm^2 mg^{-1}.

The inconsistency of item a. is solved if the calibration factor of the pulsed laser power-to-LET relation was larger than the nominal value by a factor of 1.6. On the other hand, the inconsistency of item b. is solved if the calibration factor was smaller by a factor of 0.79. Thus, these inconsistencies are contradictory.

On possible reason is the difference of the spatial distribution of the induced charge between the heavy ion and the pulsed laser. Also, it could come from the incompleteness of the pulsed laser tests, in which the SEU vulnerable spots were searched manually. Therefore, we think that it is not a serious problem.

The large inconsistency of the laser SEL result with measurements by Osborn et al.[3] is not understood.

3.2 Estimation of SEU rates during the GLAST life in orbit

We estimate here the expected SEU rates in the GLAST LAT Tracker front-end electronics based on the beam-test results. LET spectra of heavy ions on the GLAST orbit were obtained from the CREME96 program [4] assuming the planned flight orbit and the expected solar activity. Figure 11 shows the LET spectra obtained for galactic cosmic rays at the solar-minimum phase and for a solar flare event on the worst day. We utilized the SEU cross section—LET relations derived in our test (Figure 7), averaged over 0-to-1 and 1-to-0 upsets for each register block, where values between the data points were interpolated by linear fits and the values above and below the tested LET area were extrapolated by those at the maximum (= 85.6 MeV cm^2 mg^{-1}) and the minimum (= 2.81 MeV cm^2 mg^{-1}). Also, we assume a depth of the SEU sensitive volume on the chip to be 0.5 μm.

Table 3 summarizes the SEU rates obtained from the CREME96 program and the extrapolated total number of SEUs in the front-end ASICs of the entire LAT tracker (137 relevant register bits per 64-channel chip) during a ten-year operational life.

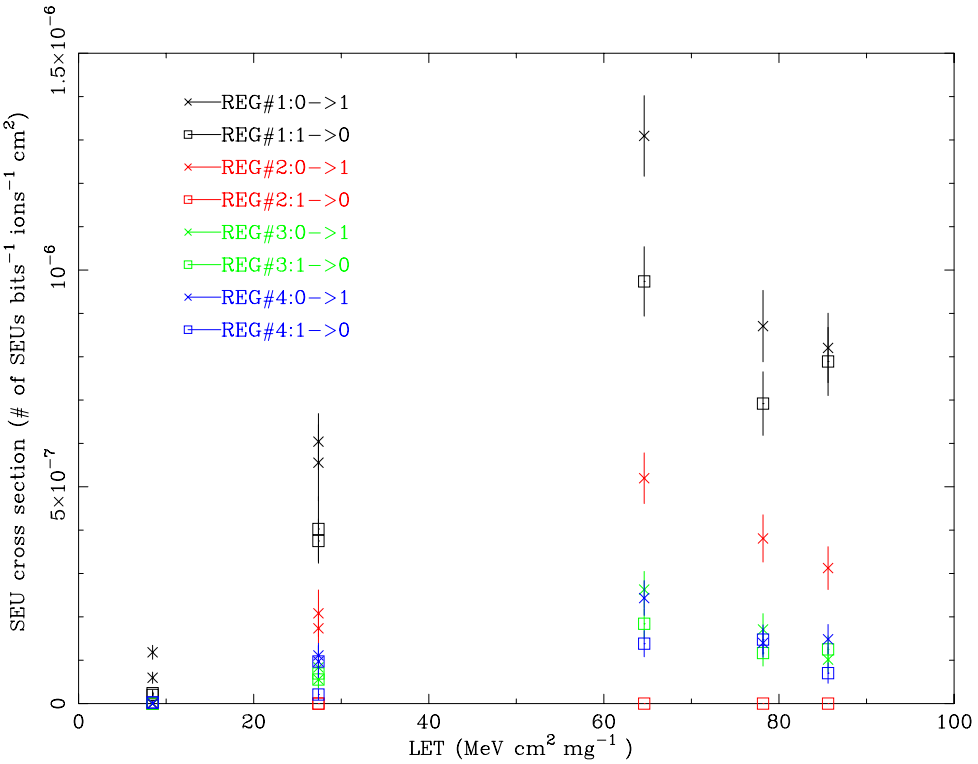

Figure 9: SEU cross section—LET relation (linear-scale plot).

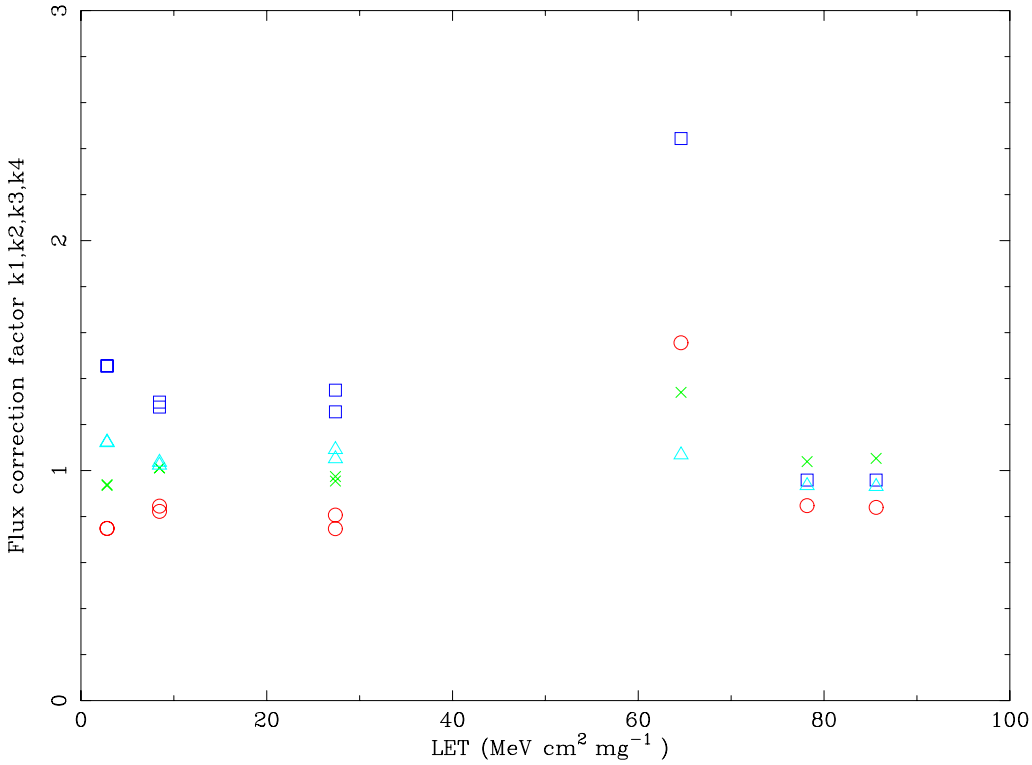

Figure 10: Distribution of the flux correction factor.

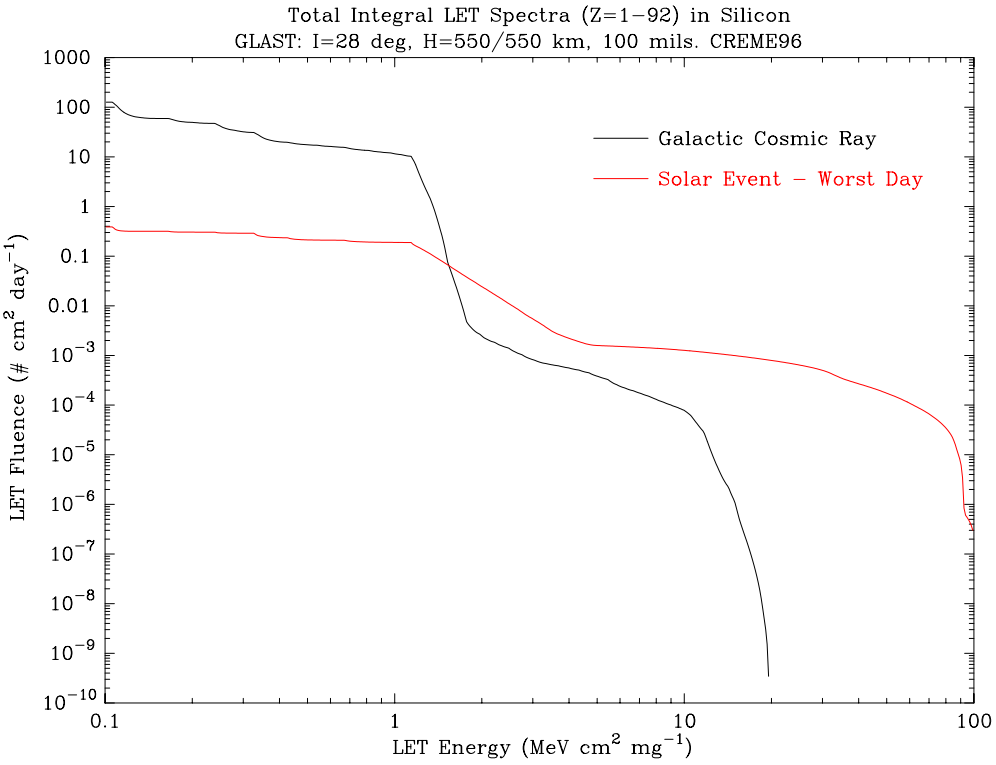

Figure 11: LET spectra

Acknowledgments

We thank Dr. S. Buchner for his help and suggestion in the pulsed laser test at NRL.

References

[1] J. Wyss, D. Bisello and D. Pantano, "SIRAD: an irradiation facility at the LNL Tandem accelerator for radiation damage studies on semiconductor detectors and electronic devices and systems", Nucl. Instr. and Meth. A 462, pp. 426-434, 2001

[2] S. Buchner, D. McMorrow, J. Melinger, and A. B. Campbell, "Laboratory Tests for Single-Event Effect", IEEE Trans. Nucl. Sci., vol.43, No. 2, pp678-686, 1996.

[3] J. Osborn et al., "Single Event Latchup Characteristics of Three Commercial CMOS Processes," 7th NASA Symposium on VLSI Design, 1998.

[4] `http://crsp3.nrl.navy.mil/creme96/`

A Latchup detection circuit

A.1 Purpose and Test

It is not necessarily easy to know whether latchups happen in CMOS circuits because various elements within and outside of the chip, including the circuits for latchup detection, could affect the status of the latchup. Thus, for R&D of our latchup detection system, we made a latchup-simulator and latchup-detection circuits and tried to observe latchup events. Figure 12 shows the schematic drawing of the latchup-simulator and the latchup detection circuits. We examined two methods to detect latchup: (A) voltage monitor and (B) current monitor, shown in Figure 12. Either of these was alternatively connected to the test circuit. We also researched what parameters affect the latchup effectively by changing parts such as resistors and capacitors in the circuits and the voltage of the power line.

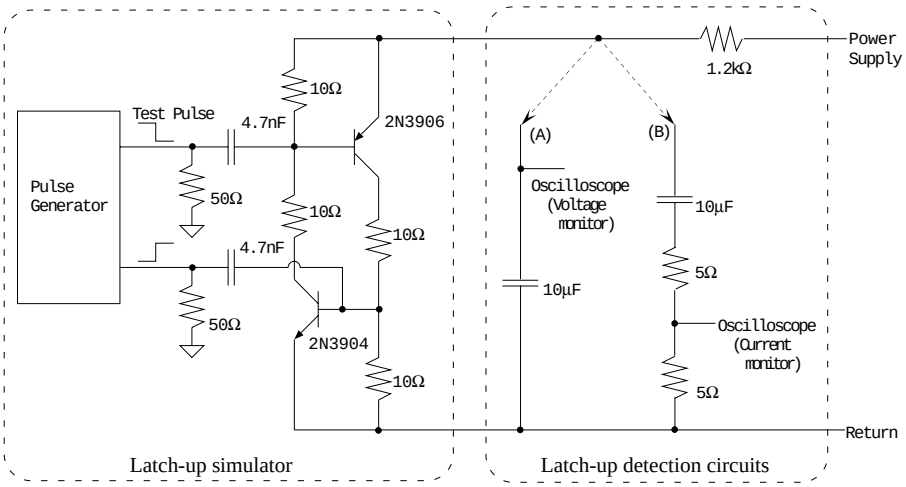

Figure 12: Schematic diagram of latchup simulation circuit and latchup detection systems.

A.2 Results

Figure 13 shows the observed waveforms of simulated latchup signals by (A) voltage monitor systems. These data were obtained in a condition of $V_{\mathrm{PowerSupply}} = 2.5$ V and $V_{\mathrm{TestPulse}} = 2.0$ V. Figure 13, left panel, shows the whole profile and the right panel shows the detail during the time that the voltage is decreasing rapidly. We can see in the left panel that the voltage decreases rapidly just after latchup happens and recovers in a time scale of $CR = 10\mu\mathrm{s} \cdot 1.2\mathrm{k}\Omega = 12\mathrm{ms}$. Also, we can estimate the current at the latchup state, I_{Latch}, from the rate of voltage decrease, which can be read in the right panel. It is approximately

$$I_{\mathrm{Latch}} = C \cdot (-dV/dt) \approx 10\mu\mathrm{F} \cdot (0.5\mathrm{V}/25\mu\mathrm{s}) = 200\mathrm{mA}. \quad (1)$$

The latchup-holding current should be one of unique parameters, depending on the property of each silicon device.

On the other hand, Figure 14 shows the observed waveforms of simulated latchup signals by (B) current monitor systems. These data were obtained in a condition of $V_{\mathrm{PowerSupply}} = 4.0$ V and $V_{\mathrm{TestPulse}} = 2.5$ V. We cannot observe latchups at $V_{\mathrm{PowerSupply}} \lesssim 3.5$ V in this system. It is reasonable, considering the fact that the voltage drop at the load resistor ($5\Omega \times 2$) for the current monitor is twice that observed, $\approx 2\times$ 1.0 V = 2.0 V. In that case, the collector-emitter voltage of paired transistors in the latchup simulator is less than 1.5 V, which is not enough to operate the transistors. The latchup current is easily estimated from the voltage drop during the latchup, $I_{\mathrm{Latch}} = 1.0\mathrm{V}/5\Omega = 200\mathrm{mA}$, which is consistent with that estimated in the voltage monitor system (equation 1).

A.3 Discussion: which kind of latchup monitor systems should we use?

We examined two kinds of latchup monitor systems: one is a voltage monitor system and the other is a current monitor system.

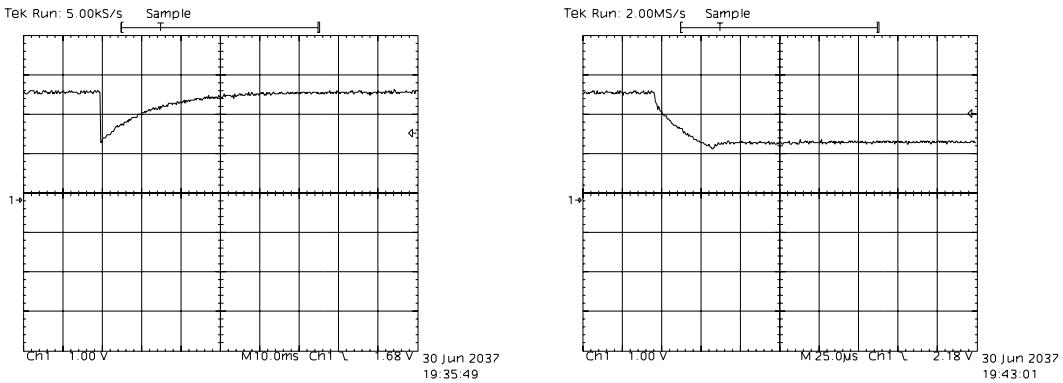

Figure 13: Observed waveforms of simulated latchup signals by (A) voltage monitor system.

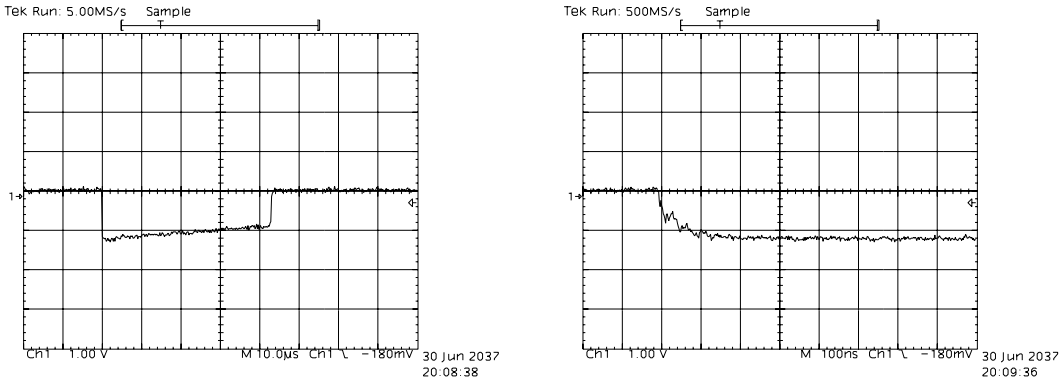

Figure 14: Observed waveforms of simulated latchup signals by (B) current monitor system.

The current monitor system is considered to make a more direct observation of latchups and seems to be much more generally used in the latchup study than the voltage monitor system. However, in the current monitor system, the voltage applied to the monitoring devices depends on the latchup current. If the minimum latchup current were higher than the limit determined by the load resistance of the current monitor, we would miss the latchup.

On the other hand, the voltage monitor system is good at a point where the voltage applied to the device is little changed, as long as an effective amount of charge on the capacitor has not been discharged as the lathcup current. The detectable limit on the lathcup current, detemined by an interior impedance of the capacitor, should be enough large. Thus, it seems to be good for the purpose of our experiments. However, the voltage monitor is considered to be more sensitive to noise.

Taking account of these facts, we adopted the voltage monitor system for the ion-beam latchup test of the LAT front-end ASIC.

Table 4: SEU-vulnerable spots in the four tested bits discovered in the NRL laser-beam test.

Register type	Tested bit-address	Upset mode	Spot ID	SEU threshold	
				Absorbed energy* (pJ)	Equivalent LET (MeV cm^2 mg^{-1})
REG#1	20	0→1	4A	> 33.3	> 100.0
			4B	3.56	10.7
			4C	35.6	106.7
REG#2	61	1→0	3A	155.5	466.6
REG#3	93	1→0	2A	> 33.3	> 100.0
			2B	1.78	5.33
			2C	24.4	73.3
			2D	22.2	66.7
REG#4	122	0→1	1A	33.3	100.0
			1B	1.33	4.0
			1C	1.78	5.33

*) Absorbed energy is estimated under assumption of 66 % transmission of laser beam energy through the passivation layer of the chip.

B SEE test by pulsed laser system at NRL

We performed SEE tests with a pulsed laser system at NRL [2] on June 28, 2001 to check the test system and obtain information on what to expect for the heavy-ion beam tests at INFN Legnaro.

B.1 SEL result

No latchups were observed in the shift register section up to 200 pJ injection, which is equivalent to an LET of 600 MeV cm^2 mg^{-1}. Other sections were not tested because they are covered by a metal layer. We also tested without any protection resistance on the power line, bu we never observed any latchup.

B.2 SEU result

Four bits in the shift register were tested for their SEU-vulnerability by an 800-nm pulsed laser beam: 20th bit, 61st, 93rd, and 122nd. The entire area of each bit was scanned with a defocused laser beam at first. Then, vulnerable spots were located by a focused beam (a beam diameter of approximately 1 μm). The SEU thershold of the spot was then sought by changing the laser intensity with the ND filter and the double-polarizer attenuator.